IN THE CLAIMS:

Claims 1-79. (Canceled)

80. (Currently amended) A processor for operating certain data in accordance with an instruction in a program, comprising:

a first register unit;

a second register unit;

a sign-extending unit;

a zero extending unit,

wherein said zero-extending unit zero-extends data when the instruction designates said first register unit and said sign-extending unit sign-extends data when the instruction designates said second register unit.

81. (Previously presented) The processor of Claim 80, wherein the instruction includes a destination operand which designates one of said first register unit and said second register unit.

82. (Previously presented) The processor of Claim 81, wherein said data is an immediate data included in the instruction.

83. (Currently amended) A processor for operating certain data in accordance with an instruction in a program, comprising:

a first register unit;

a second register unit;

a sign-extending unit;

a zero-extending unit; and

an instruction decoding unit for decoding an instruction in the program to detect a first type instruction and a second type instruction, said first type instruction including an instruction to store data into said first register unit, said second type instruction including an instruction to store data into said second register unit, with said first type instruction and said second type instruction having a different destination operand to designate whether to store data into said first register unit or said second register unit;

wherein said zero-extending unit zero-extends data when a first type instruction is detected and said sign-extending unit sign-extends data when a second type instruction is detected.

84. (Previously presented) The processor of Claim 83, wherein said data is an immediate data included in the first type instruction and the second type instruction.

85. (Currently amended) A data processing method for executing an instruction that designates one of a first register and a second register, said method comprising:

decoding the instruction for selecting one of the first register and the second register in accordance with an operand of the decoded instruction;

zero-extending data when said decoded instruction designates the first register; and

sign-extending data when said decoded instruction designates the second register.

86. (Previously presented) The data processing method of Claim 85, wherein the operand is a destination operand which designates one of the first register and the second register.

87. (Previously presented) The data processing method of Claim 86, wherein said data is an immediate data included in the instruction.

88. (Currently amended) A processor for operating certain data in accordance with an instruction, comprising:

a first register unit;

a second register unit;

a processing unit configured to process zero-extending data when the instruction designates the first register and to process sign-extending data when the instruction designates the second register.

89. (Previously presented) The processor of Claim 88, wherein the instruction includes a destination operand which designates either the first register unit or the second register unit.

90. (Previously presented) The processor of Claim 89, wherein the data is an immediate data.

91. (Currently amended) A data processing method for executing an instruction that designates one of a first register and a second register, said method comprising:

decoding the instruction;

processing zero-extending data when the instruction designates the first register; and

processing sign-extending data when the instruction designates the second register.

92. (Previously presented) The method of claim 91, wherein said instruction includes a destination operand which designates either the first register unit or the second register unit.

93. (Previously presented) The method of claim 92, wherein said data is an immediate data.

94. (Currently amended) The processor for executing instructions, comprising:

a first register unit;

a second register unit;

a first processing unit; and

a second processing unit;

wherein an instruction directs the first processing unit to perform zero-extending when the instruction designates the first register unit and directs the second processing unit to perform sign-extending when the instruction designates the second register unit.